

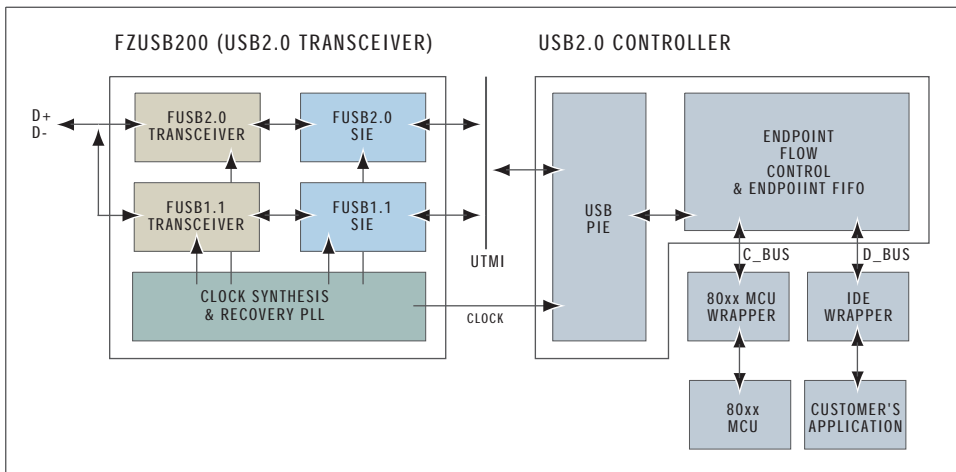
FARADAY TECHNOLOGY CORPORATION

# FZUSB200: USB2.0 TRANSCEIVER

Faraday's FZUSB200 is a USB2.0 transceiver IP that fully complies with USB2.0 specification. Faraday's USB2.0 transceiver IP core supports a high-speed transfer rate of 480Mbps, while it is also backward compatible with USB1.1 full-speed (12Mbps) and low speed (1.5Mbps) transfer rate. The accelerated data rate improves the performance dramatically for applications that require high speed data transferring, such as mass storage devices, real-time multimedia devices, gaming devices, communication devices, scanners, printers, digital cameras, PDAs, and many others.

FZUSB200 is initially developed for UMC 0.25µm CMOS process and it can be easily mapped into more advanced process technology. The digital interface of FZUSB2.0 follows Intel's USB2.0 Transceiver Macrocell Interface (UTMI) specification (version 1.05) and supports both 8-bit/60MHz and 16-bit/30MHz bus interfaces. It can be easily integrated with Faraday's USB2.0 device controller IP, FUSB200, or a customer's device controller that follows UTMI standard.

## SYSTEM BLOCK DIAGRAM



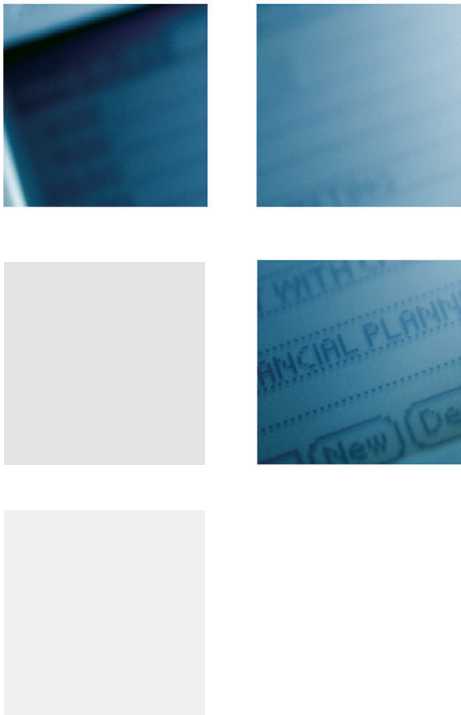
Faraday's USB2.0 transceiver IP FZUSB200 includes five distinct blocks: the clock synthesis/recovery phase locked loop (PLL) block, USB2.0/1.1 mixed-signal transceiver blocks, and USB2.0/1.1 serial interface engine (SIE) blocks.

The PLL block provides current references and generates 480MHz clock signals to mixed-signal transceiver blocks and digital SIE blocks. The USB2.0/1.1 mixed-signal transceiver blocks contain the analog drivers, receivers, and data recovery modules. The USB2.0/1.1 digital SIE blocks send and receive data between transceivers and USB2.0 link layer logic through UTMI. SIE blocks also control the mixed-mode modules for proper speed mode termination.

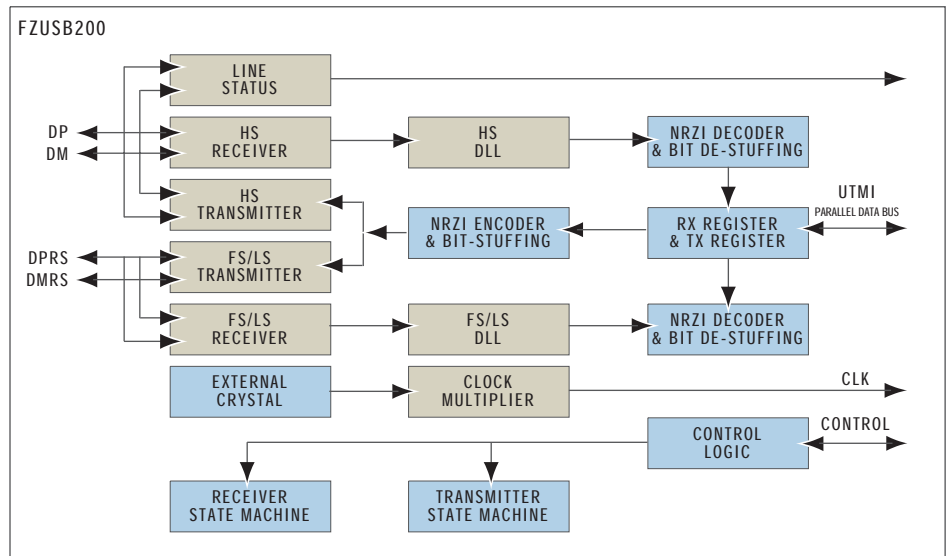
Faraday also provides customers with a state-of-the-art USB2.0 device controller IP, named as FUSB200. For more information regarding Faraday's FUSB200, please refer to its product brief.

## FEATURES

- 480Mbps high speed data rate
- Backward compatible to USB1.1 full speed (12Mbps) and low speed (1.5Mbps)
- Intel UTMI compliant
- Integrated bit stuffing and unstuffing
- NRZI encoding and decoding
- USB data receiving recovery
- Synchronized USB data transmission
- 3.3V for mixed-signal logic
- 2.5V for digital logic
- Easy to integrate
- Low power consumption
- Build-in Self Test (BIST) function



## FUNCTIONAL BLOCK DIAGRAM



Faraday's FZUSB200 design architecture is very compact and robust. While transmitting data packets, the FZUSB200 transceiver receives parallel data from UTMI, serializes the data, performs bit stuffing and non-return-to-zero-inverted (NRZI) encoding, attaches the SYNC and EOP fields and transfers to the peer USB device through the USB cable.

Likewise, while receiving incoming data packets, FZUSB200 transceiver IP locks the USB signaling, detects and strips the SYNC, EOP fields, performs NRZI decoding and bit unstuffing, parallelizes and transfers to UTMI interface.

FZUSB200 offers two configurations: one is a 16-bit bus operating at 30MHz, the other is an 8-bit bus operating at 60MHz. The lower speed feature of the 16-bit bus allows easier implementation in an FPGA verification stage, while the 8-bit bus can reduce the gate count thus reducing the cost for ASIC designs.

## ABOUT FARADAY

Faraday Technology Corporation provides ASIC design services and IPs for customers ranging from small start-ups to large multinational corporations. With over 1,200 successful tapeouts since 1996, Faraday is your best SoC design partner that always ensures time-to-market while minimizing the development risk and cost. Headquartered in Hsinchu, Taiwan, Faraday has branch offices around the world, including Japan, China, Europe and the U.S.

## DELIVERABLES

- GDSII layout data
- Timing model
- DRC, LVS command files
- P&R abstract model
- LVS netlist
- Testbench and behavioral model
- Test chip
- Product datasheet
- Application notes

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